Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1. (currently amended) An instruction fetch unit for a processor, comprising:

a first recoder; and

a second recoder coupled to the first recoder,

wherein the first recoder passes information regarding a first instruction to the second recoder, and the second recoder recodes a second instruction so as to map the second instruction from a first encoded state to a second encoded state based on the information passed by the first recoder.

2. (original) The instruction fetch unit of claim 1, further comprising:

an instruction-staging unit coupled to the first recoder and the second recoder that dispatches an instruction from an instruction cache to one of the first recoder and the second recoder.

3. (original) The instruction fetch unit of claim 1, wherein the processor executes instructions having X-bits and belonging to a first instruction set and instructions having Y-bits and belonging to a second instruction set, Y being greater than X, and wherein the first recoder and the second recoder recode an instruction belonging

to one of the first instruction set and the second instruction set to form a recoded instruction having at least Y-bits.

4. (original) The instruction fetch unit of claim 3, wherein each instruction of the first instruction set has 16-bits and each instruction of the second instruction set has 32-bits.

5. (original) The instruction fetch unit of claim 3, wherein the first instruction set includes an expand instruction used to enlarge an immediate field of an expandable instruction of the first instruction set, and wherein the first recoder passes at least one bit of the expand instruction to the second recoder thereby allowing the second recoder to recode the expandable instruction.

6. (original) The instruction fetch unit of claim 5, wherein the at least one bit of the expand instruction is concatenated to at least one bit of the expandable instruction.

7. (original) The instruction fetch unit of claim 3, wherein the first instruction set includes a mode-switching instruction that switches the operating mode of the processor, and wherein the first recoder passes one or more bits to the second recoder thereby allowing the second recoder to recode the mode-switching instruction.

8. (original) The instruction fetch unit of claim 7, wherein the one or more bits are concatenated to at least one bit of the mode-switching instruction.

9. (currently amended) A processor, comprising:

a first recoder; and

a second recoder coupled to the first recoder,

wherein the first recoder passes information regarding a first instruction to the second recoder, and the second recoder recodes a second instruction so as to map the second instruction from a first encoded state to a second encoded state based on the information passed by the first recoder.

10. (original) The processor of claim 9, further comprising:

an instruction-staging unit coupled to the first recoder and the second recoder that dispatches an instruction from an instruction cache to one of the first recoder and the second recoder.

11. (original) The processor of claim 10, wherein the processor executes instructions having X-bits and belonging to a first instruction set and instructions having Y-bits and belonging to a second instruction set, Y being greater than X, and wherein the first recoder and the second recoder recode an instruction belonging to one of the first instruction set and the second instruction set to form a recoded instruction having at least Y-bits.

12. (original) The processor of claim 11, wherein each instruction of the first instruction set has 16-bits and each instruction of the second instruction set has 32-bits.

13. (original) The processor of claim 11, wherein the first instruction set includes an expand instruction used to enlarge an immediate field of an expandable instruction of the first instruction set, and wherein the first recoder passes at least one bit of the expand instruction to the second recoder thereby allowing the second recoder to recode the expandable instruction.

14. (original) The processor of claim 13, wherein the at least one bit of the expand instruction is concatenated to at least one bit of the expandable instruction.

15. (original) The processor of claim 11, wherein the first instruction set includes a mode-switching instruction that switches the operating mode of the processor, and wherein the first recoder passes one or more bits to the second recoder thereby allowing the second recoder to recode the mode-switching instruction.

16. (original) The processor of claim 15, wherein the one or more bits are concatenated to at least one bit of the mode-switching instruction.

17. (currently amended) A processing system, comprising:

a first recoder for generating at least one information bit based on an expand instruction; and

a second recoder, coupled to the first recoder, for recoding an expandable instruction so as to map the expandable instruction from a first encoded state to a second encoded state based on the at least one information bit from the first recoder.

18. (original) The processing system of claim 17, further comprising:

an instruction-staging unit coupled to the first recoder and the second recoder that dispatches an instruction from an instruction cache to one of the first recoder and the second recoder.

19. (original) The processing system of claim 17, wherein the processing system executes instructions having X-bits and belonging to a first instruction set and instructions having Y-bits and belonging to a second instruction set, Y being greater than X, and wherein the first recoder and the second recoder recode an instruction belonging to one of the first instruction set and the second instruction set to form a recoded instruction having at least Y-bits.

20. (previously presented) The processing system of claim 19, wherein each instruction of the first instruction set has 16-bits and each instruction of the second instruction set has 32-bits.

21. (previously presented) The processing system of claim 19, wherein the expand instruction is used to enlarge an immediate field of the expandable instruction, and wherein the first recoder passes expand field bits to the second recoder.

22. (previously presented) The processing system of claim 21, wherein the expand field bits are concatenated to at least one bit of the expandable instruction.

23. (currently amended) A tangible computer readable storage medium comprising a microprocessor core embodied in software, the microprocessor core comprising:

a first recoder; and

a second recoder coupled to the first recoder,

wherein the first recoder passes information regarding a first instruction to the second recoder, and the second recoder recodes a second instruction so as to map the second instruction from a first encoded state to a second encoded state based on the information passed by the first recoder.

24. (previously presented) The tangible computer readable storage medium of claim 23, further comprising:

an instruction-staging unit coupled to the first recoder and the second recoder that dispatches an instruction from an instruction cache to one of the first recoder and the second recoder.

25. (previously presented) The tangible computer readable storage medium of claim 23, wherein the microprocessor core executes instructions having X-bits and belonging to a first instruction set and instructions having Y-bits and belonging to a second instruction set, Y being greater than X, and wherein the first recoder and the second recoder recode an instruction belonging to one of the first instruction set and the second instruction set to form a recoded instruction having at least Y-bits.

26. (previously presented) The tangible computer readable storage medium of claim 25, wherein each instruction of the first instruction set has 16-bits and each instruction of the second instruction set has 32-bits.

27. (previously presented) The tangible computer readable storage medium of claim 25, wherein the first instruction set includes an expand instruction used to enlarge an immediate field of an expandable instruction of the first instruction set, and wherein the first recoder passes at least one bit of the expand instruction to the second recoder thereby allowing the second recoder to recode the expandable instruction.

28. (previously presented) The tangible computer readable storage medium of claim 27, wherein the at least one bit of the expand instruction is concatenated to at least one bit of the expandable instruction.

29. (previously presented) The tangible computer readable storage medium of claim 25, wherein the first instruction set includes a mode-switching instruction that switches the operating mode of the processor, and wherein the first recoder passes one or more bits to the second recoder thereby allowing the second recoder to recode the mode-switching instruction.

30. (previously presented) The tangible computer readable storage medium of claim 29, wherein the one or more bits are concatenated to at least one bit of the mode-switching instruction.

31. (currently amended) A method for recoding instructions for execution by a processor, comprising:

(a) fetching an expand instruction and an expandable instruction ~~from an instruction cache~~;

(b) dispatching the expand instruction ~~to a first recoder~~ and ~~dispatching~~ the expandable instruction ~~to a second recoder~~;

(c) generating ~~at the first recoder~~ at least one information bit based on the expand instruction; and

(d) recoding the expandable instruction ~~at the second recoder~~ using the at least one information bit generated ~~at the first recoder~~ so as to map the expandable instruction from a first encoded state to a second encoded state.

32. (previously presented) The method of claim 31, wherein step (a) comprises:

(i) fetching the expand instruction during a first clock cycle of the processor; and

(ii) fetching the expandable instruction during a subsequent clock cycle of the processor.

33. (currently amended) The method of claim 31, wherein the at least one information bit based on the expand instruction is generated ~~at the first recoder~~ during a first clock cycle of the processor, and the expandable instruction is recoded ~~at the second recoder~~ during a second clock cycle of the processor.

34. (currently amended) The method of claim 33, further comprising a step between steps (c) and (d) of:

storing the at least one information bit ~~generated at the first recoder~~ in an information storage buffer.

35. (currently amended) A method for recoding instructions for execution by a processor, comprising:

fetching a plurality of instructions from an instruction cache, wherein the plurality of instructions includes a first instruction and a second instruction, and the first instruction is different from the second instruction;

dispatching the first instruction to a first recoder and the second instruction to a second recoder; and

recoding the first instruction and the second instruction[[s]] within a single clock cycle so as to map each of the first instruction and second instruction from a first encoded state to a second encoded state.

36. (currently amended) The method of claim 35, wherein the recoding of the second instruction is performed using information from the first ~~instruction~~ recoder.

37. (currently amended) The method of claim 35, further comprising forwarding ~~information~~ at least one bit from the first recoder to the second recoder, ~~such information~~ wherein the at least one bit is used by the second recoder to perform a recoding operation.

38. (currently amended) An instruction fetch unit for a processor comprising:

~~a first recoder; and~~

a ~~second recoder which~~ plurality of recoders that operate[[s]] in parallel ~~with the first recoder~~;

wherein the ~~first~~ recoders recode[[s]] ~~a first instruction and the second recoder recodes a second~~ instructions within a single clock cycle so as to map the instructions from a first encoded state to a second encoded state. ~~, and the first instruction is different from the second instruction.~~

39. (currently amended) The instruction fetch unit of claim 38, wherein ~~the second~~ one of the recoders recodes one ~~the second~~ instruction using information from ~~the first instruction~~ another recoder.

40. (currently amended) The instruction fetch unit of claim 39, wherein the ~~first recoder is coupled to the second recoder~~ information includes at least one bit.

41. (original) The instruction fetch unit of claim 1, wherein the first instruction is used to enlarge a field of the second instruction and the information is at least one bit of the first instruction.

42. (original) The instruction fetch unit of claim 41, wherein the first instruction is an expand instruction, the second instruction is an expandable instruction and the field is an immediate field.

43. (original) The processor of claim 9, wherein the first instruction is used to enlarge a field of the second instruction and the information is at least one bit of the first instruction.

44. (previously presented) The processor of claim 43, wherein the first instruction is an expand instruction, the second instruction is an expandable instruction and the field is an immediate field.

45. (previously presented) The tangible computer readable storage medium of claim 23, wherein the first instruction is used to enlarge a field of the second instruction and the information is at least one bit of the first instruction.

46. (previously presented) The tangible computer readable storage medium of claim 45, wherein the first instruction is an expand instruction, the second instruction is an expandable instruction and the field is an immediate field.